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Fundamental Physical Aspects of Carbon Nanotube Transistors

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1. Introduction

The increasing demand for ultra-high speed processors, smaller dimensions and lower power consumption of integrated circuits has made the technology scaling of the electronic components a challenging issue for device designers. In past few decades, miniaturization of transistors has always obeyed the moore's law: the number of transistors that can be placed inexpensively on an integrated circuit has doubled approximately every two years. Nanoscale field effect transistors in the sub-10 nm regime, suffer from short channel effects such as direct tunneling from source to drain, increase in gate-leakage current and punch-through effect. These effects have posed severe problems for miniaturized transistors and directed the recent research toward better alternative semiconductors than silicon. Semiconducting carbon nanotubes (CNTs) because of their properties like large mean free path, excellent carrier mobility and improved electrostatics at nanoscales as the result of their non-planar structure, have been known as the best ideal replacement for silicon. In particular, they exhibit ballistic transport over length scales of several hundred nanometers (Heinze, et al., 2006). Absence of the dangling bond states at the surface of CNTs and purely one-dimensional transport properties improve gate control while meeting gate leakage constrains and allows for a wide choice of gate insulators. That's why CNTs suppress the short channel effects in transistor devices. Symmetry of the conduction and valence bands makes CNTs advantageous for complementary applications. CNTs are very attractive for nanoelectronic applications and can be used to achieve high speed ballistic carbon nanotube field effect transistors (CNTFETs). Theoretically, CNTFETs could reach a higher frequency domain (terahertz regime) than conventional semiconductor technologies. CNTFETs, only a few years after the initial discovery of CNTs in 1991 by Sumio Iijima (Iijima, 1991) were first demonstrated in 1998 by Dekker et al. at Delft University (Tans, et al., 1998) and soon after by groups at IBM (Martel, et al., 1998) and Stanford University (Soh, et al., 1999). Intensive research has led to a significant progress in understanding the fundamental properties of CNTs. By using a single-wall CNT as the channel between two electrodes which work as the source and drain contacts of a FET, a coaxial CNTFET can be fabricated. Coaxial devices are of special interest because their geometry allows for better electrostatics because the gate contact wraps all around the channel (CNT) and has a very good control on carrier

transport. Type of Metal-CNT contacts plays crucial role in the output characteristics of the transistor. Heavily doped semiconductors because of the ability to form Ohmic contacts can be used as ideal electrodes but they suffer from high parasitic resistance. Existence of potential barrier at the metal-CNT interface, changes the device to a CNTFET resembling to Schottky barrier MOSFETs. However, heavily doped CNT contacts can be used to get to a behavior similar to conventional MOSFETs.

Understanding CNTFETs from electronic point of view requires a deep insight for mesoscopic physics. For modelling a CNTFET, a powerful methodology with the abilities of solving Schrödinger equation under non-equilibrium conditions in the presence of self-consistent electrostatics and treating coupling of the channel to contacts is needed. The non-equilibrium Green's function (NEGF) formalism provides a sound basis for quantum device simulations. In this chapter we aim to introduce different types of CNTFETs, their electrostatics and output characteristics.

The chapter is organized as follows: section 2 introduces different types of CNTFETs and typical design parameters, section 3 explains different physical issues involved with CNTFETs and ultimately in section 4 we briefly describe the NEGF formalism and WKB treatment for simulating CNTFETs. We use these methods to plot the curves for implying physical aspects through the chapter. While explaining the important issues, new challenges for achieving a well-designed CNTFET will be explained. After reading this chapter, the reader should be able to distinguish how a specific type of CNTFETs behaves (both DC analysis and high frequency response) and why.

2. Common CNTFET Designs

2.1 Types of CNTFETs

There are two main types of CNTFETs that are being currently studied, differing by their current injection methods. CNTFETs can be fabricated with Ohmic or Schottky contacts. The type of the contact determines the dominant mechanism of current transport and device output characteristics. CNTFETs are mainly divided into Schottky barrier CNTFETs (SB-CNTFETs) with metallic electrodes which form Schottky contacts and MOSFET-like CNTFETs with doped CNT electrodes which form Ohmic contacts. In SB-CNTFETs, tunneling of electrons and holes from the potential barriers at the source and drain junctions constitutes the current. The barrier width is modulated by the application of gate voltage, and thus, the transconductance of the device is dependent on the gate voltage (Raychowdhury, et al., 2006).

The other type of the CNTFETs takes advantage of the n-doped CNT as the contact. Potassium doped source and drain regions have been demonstrated and the behavior like MOSFETs have been experimentally verified (Javey, et al., 2005). In this type of transistors a potential barrier is formed at the middle of the channel and modulation of the barrier height by the gate voltage controls the current.

2.2 Typical Designs

At this point, we consider two typical designs for two types of the CNTFETs and use them for investigation and comparison of the transistors' behaviors. Let's consider two coaxial CNTFETs with a (13,0) zigzag CNT as the channel which corresponds to a bandgap of about 0.83 eV and a diameter of 1 nm. A 2 nm thick ZrO_2 with a relative permittivity of 25

separates the gate electrode and the CNT. The gate is 10 nm long and wrapped around the channel. The gate thickness is assumed 6 nm. SB-CNTFET employs an intrinsic CNT and 20 nm long metallic contacts as the source and drain. A typical structure and the distribution of the potential energy on the channel are shown in figure 1. The gate voltage makes the barriers near the source/drain thinner and increases the tunneling current.

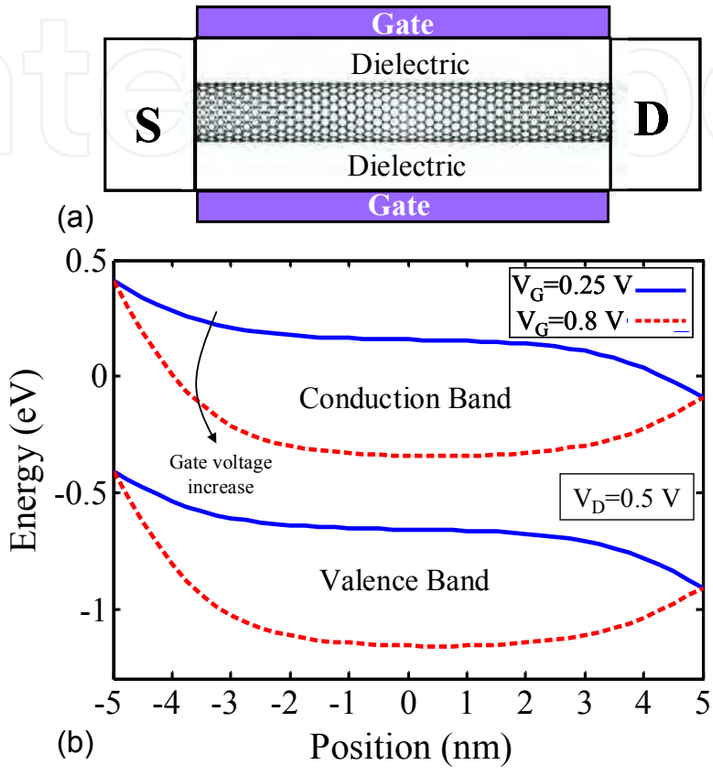

Fig. 1. Schottky Barrier CNTFET, a) 2-D cross section of the coaxial structure with intrinsic CNT as the channel and metal source/drain contacts, b) Energy band diagram obtained from Poisson equation. The metal Fermi level is taken to be at the midgap of the CNT.

On the other hand the MOSFET-like CNTFET benefits from heavily doped ends of the CNT which act as Ohmic source and drain contacts. A typical structure of the MOSFET-like CNTFETs with 20 nm doped sections and its energy band diagram is shown in figure 2. The source/drain doping is 10^{-9} m^{-1} (~0.01 dopant per atom). In the following sections of this chapter these two transistors will be compared to each other and the results can be generalized to other designs. The curves of this chapter have been obtained using the described methods in section 4.

3. Important Aspects of CNTFETs

3.1 Ambipolarity

One of the important aspects of nanotube transistors is the ambipolarity or unipolarity of their current-voltage characteristics. SB-CNTFETs exhibit strong ambipolar behavior. For high enough gate voltages the tunneling probability of electrons through the source

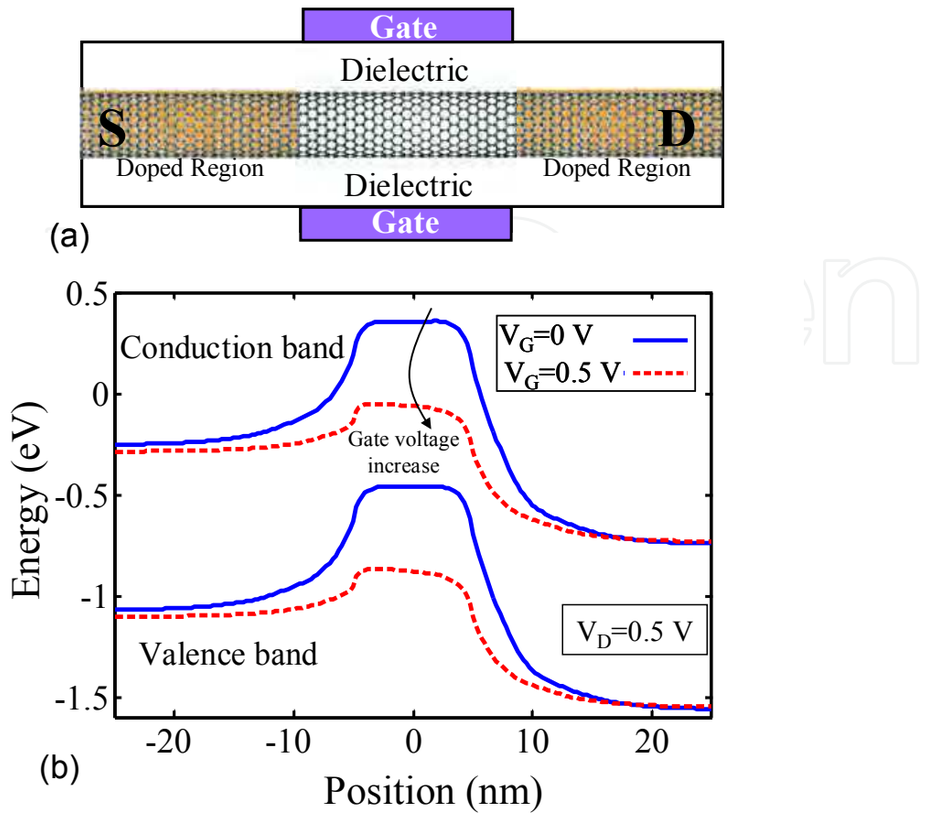

Fig. 2. MOSFET-like CNTFET, a) 2-D cross section of the coaxial structure with intrinsic CNT as the channel and doped CNT sections as source/drain contacts , b) Energy band diagram obtained from Poisson equation.

Schottky barrier in the conduction band is high and for the low and negative gate voltages, a Schottky barrier is formed at the drain in valence band and tunneling of holes increases the current. The energy bands for low and high gate voltages and the Schottky barriers are shown in figure 1(b). However for MOSFET-like CNTFETs only positive gate voltages because of lowering the barrier in the channel increase the current. The energy bands for low and high gate voltages and the potential barrier in the channel are shown in figure 2(b). It is clear from the figures why the characteristics of these two transistors differ. The current-voltage characteristics of the devices have been compared in figure 3.

Ambipolar behavior of the SB-CNTFETs constraints the use of these transistors in conventional CMOS logic families. We have proposed some methods to reduce or eliminate the ambipolarity in CNTFETs. Using asymmetrical contact types we have introduced Schottky-Ohmic CNTFET which has a Schottky barrier at the CNT-metal interface at the source and an Ohmic contact at the drain at the channel-doped CNT interface (Kordrostami, et al., 2008). However, the device still suffers from band to band tunneling. That is, in low or negative voltages the electrons from the valence band can tunnel to the conduction band and contribute to the total current of the transistor and cause increase of the current in negative voltages. We have compared the potential energy distribution of the channel of the transistors in figure 4 (Kordrostami, 2007).

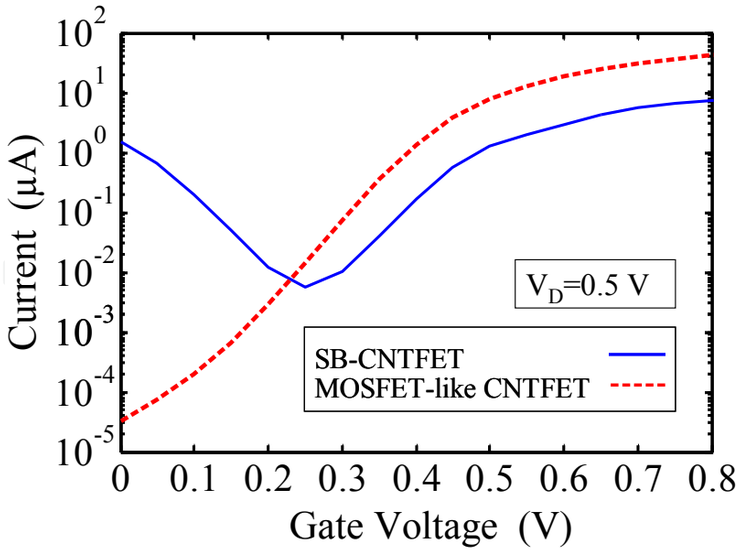

Fig. 3. Comparison between the current-voltage characteristics of the SB and MOSFET-like CNTFETs. Ambipolar behavior of the SB-CNTFET and the unipolar characteristic of the MOSFET-like CNTFET can be seen from the curves.

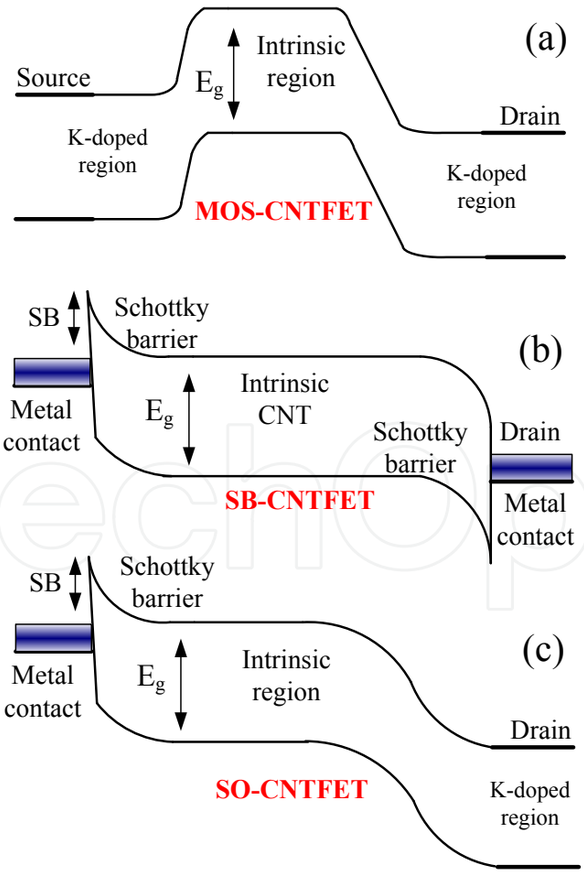

Fig. 4. Potential energy distribution along the carbon nanotube in three different CNTFET structures, a) MOSFET-like, b) Schottky barrier, c) Schottky-Ohmic (Kordrostami, 2007)

Double-gate structures can also reduce the ambipolarity while the CNT is still intrinsic. In the structure shown in figure 5 the first gate controls carrier injection at the source and the second one acts like an electrostatic doping and controls carrier injection at the drain which can be used to suppress the hole tunneling current, for example by applying the same voltage as the drain voltage to the second gate (Pourfath, et al., 2005). In this case, at any drain voltage the band edge profile near the drain contact will be flat like the band diagram in figure 4(c). On the other hand, an advantage of an ambipolar SB-CNTFETs is that they can be used as either an n-type and p-type FET in a CMOS application (Guo and Lundstrom, 2009).
In MOSFET-like CNTFETs with heavily doped source and drain regions, when applying a negative gate voltage, the band to band tunneling may lead to ambipolarity. For suppressing this effect in MOSFET-like CNTFETs we proposed a non-uniform doping profile as shown in figure 6 (Hassaninia, et al., 2008b). This reduces the gradient of the channel potential barrier at each interface between the intrinsic and doped sections of the CNT and suppresses the band to band tunneling and ambipolar conduction.

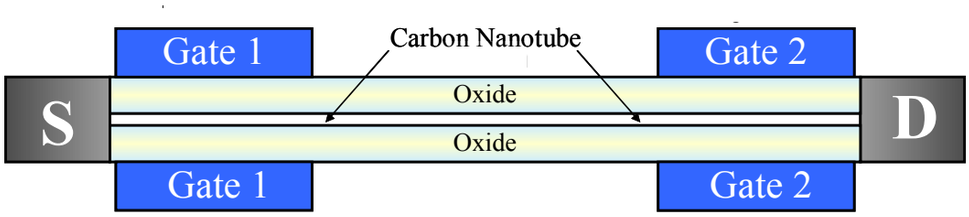

Fig. 5. Double gate CNTFET (Hassaninia, et al., 2008a). The first gate modulates the source tunneling current and the second gate in fact eliminates the Schottky barrier at the drain (path for tunneling of the holes in the valence band).

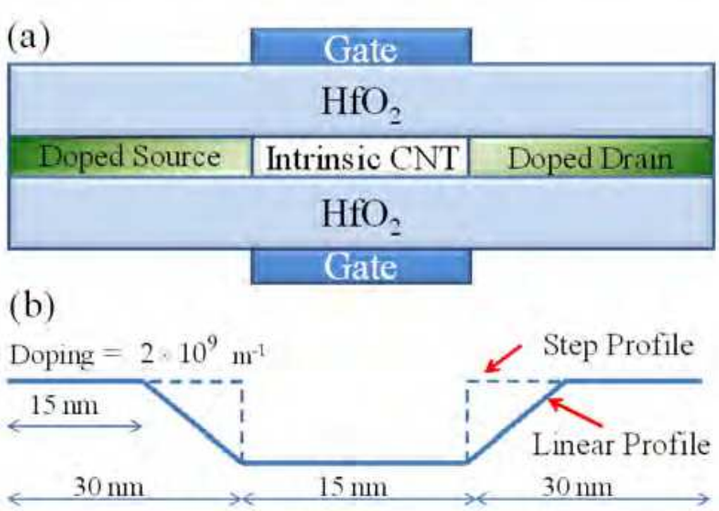

Fig. 6. a) Cross section of the CNTFET. (b) Step and linear doping profiles for the MOSFET-like structure versus position.

3.2 High Permittivity Gate Dielectrics

The relatively low dielectric constant of SiO_2 (at 3.9) limits its use in transistors as gate lengths scale down to tens of nanometers. As the device dimensions approach the 10 nm regime, strong electrostatic coupling of source/drain electrodes arises fundamental challenges especially about the gate control over the channel. Enhancing the gate efficiency requires thinner gate oxides. However, due to excessive direct tunneling leakage currents through the ultra-thin dielectric, the gate dielectric layer is already approaching its limit (~ 1nm) and the only feasible way is to use high-κ gate dielectrics which afford high gate capacitance without relying on ultra-small film thickness (Javey, et al., 2002). The most common gate oxides for nanotransistors are Zirconium[1] (ZrO_2) and Hafnium dioxide (HfO_2) with relative permittivities about 25 and 16 respectively. The current versus the dielectric constant of the oxide in both types of transistors has been shown in figure 7.

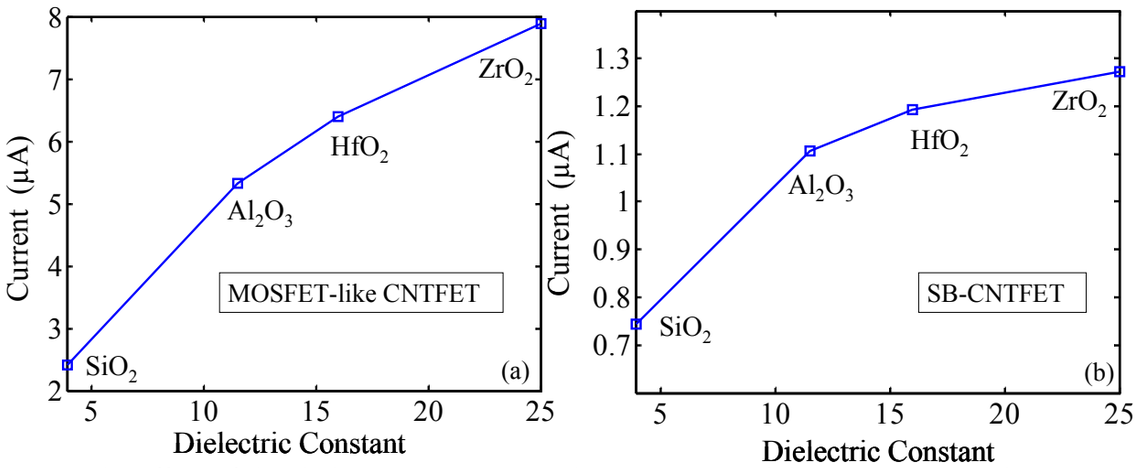

Fig. 7. The effect of the dielectric constant on the on current of the transistors in the on state. (V_G=V_D=0.5 V).

3.3 On/Off Current

Comparison shows that MOSFET-like CNTFETs due to absence of Schottky barriers have a lower off leakage current. On the other hand, in the on state, there is no barrier at the source-channel junction and hence, the device demonstrates significantly higher on current. The minimum current of the SB-CNTFETs occurs when the contribution of the electron and hole tunneling currents to the total current becomes equal, that is when $V_G = V_D/2$ where the energy band diagram is symmetric. For each power supply voltage (V_D), the off-current is defined at the minimal leakage point $V_G(off)=V_D/2$ and the on-current is defined at $V_G(on)=V_G(off)+V_D$. There exists a trade-off: reducing the off-current by lowering the power supply voltage degrades the on-current.

3.4 Transconductance

The transconductance (g_m) of the SB-CNTFETs is severely limited by the Schottky barriers in the on state. The transconductances of the devices as a function of the gate voltage have

[1] The name Zirconium originates from the Persian word 'zargun' meaning gold-like.

been compared to each other in figure 8(a). It is seen that transconductance of the MOSFET-like CNTFET is higher than the SB-CNTFET. Figure 8(b) plots CNTFET on state transconductance versus the gate dielectric constant for four types of widely used gate insulators. The high-κ gate insulator improves the CNTFET performance by reducing the self-consistent potential produced by the charge on the tube (Guo, 2004). For the SB-CNTFETs the transconductance tends to saturate when the gate insulator dielectric constant is large. The reason is that the self-consistent potential produced by the charge on the tube is already small and further improving the gate dielectric constant does not help to significantly reduce the Schottky barrier thickness and the transistor performance (Guo, 2004).

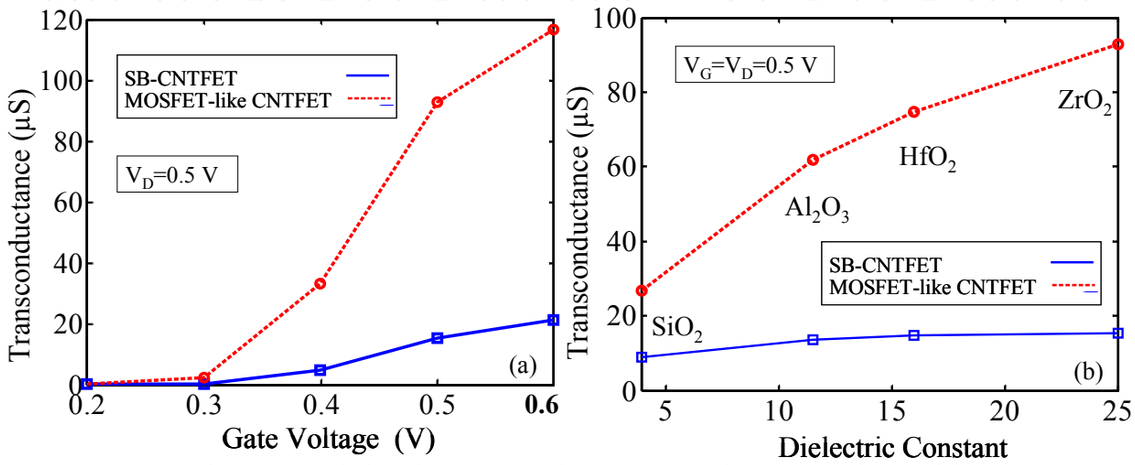

Fig. 8. Transconductance of the CNTFETs, a) g_m versus the gate voltage, b) g_m variations with respect to the dielectric constant.

3.5 Gate Capacitance

For a one dimensional nanotube FET, the total capacitance between the gate and the channel (gate capacitance) depends both on the geometry and the density of states (DOS). If the electrostatic potential on the channel (V_S) is uniform, then the voltage drop over the gate oxide is also uniform and the gate voltage V_G is the summation of the channel potential and the voltage drop over the gate oxide. This can be modeled as the potential division between two capacitances which means the gate capacitance (total capacitance) can be modeled as the series of the electrostatic (geometry dependent) capacitance and the quantum (DOS dependent) capacitance as shown in figure 9. Gate capacitance can be calculated from:

$$C_g = \partial Q / \partial V_G \tag{1}$$

where Q is the total charge on the gate electrode (which has the same magnitude but an opposite sign as the total net charge of the CNT) and V_G is the gate voltage. The gate oxide plays the role of the dielectric between the plates of the oxide (electrostatic) capacitance which can be expressed as:

$$C_{ox} = 2\pi\varepsilon L_g \Big/ Ln\left(\frac{t_{ox} + r_{CNT}}{r_{CNT}}\right) \tag{2}$$

where t_{ox} is the gate dielectric thickness, ε is the dielectric constant of the gate insulator, L_g is the gate length and r_{CNT} is the nanotube diameter. Since the charge on the channel (Q) can be derived from CNT density of states and the Fermi level for a given channel potential, the quantum capacitance can be calculated from:

$$C_q = \partial Q / \partial V_s \tag{3}$$

where V_s is the channel potential. For MOSFET-like CNTFETs V_s and Q can be defined as the potential energy and charge density at the top of the channel potential barrier.

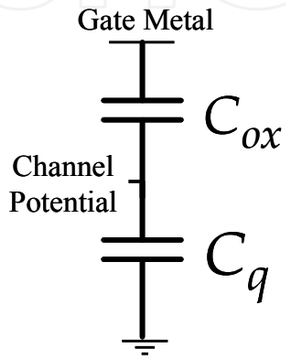

Fig. 9. Series combination of the oxide and quantum capacitances and the voltage drop on the capacitances.

The above derivation is strictly valid only when V_S is position-independent, otherwise the definition of the oxide capacitance breaks down (Guo, et al., 2007). The gate capacitances of the transistors versus the dielectric constant are shown in figure 10.

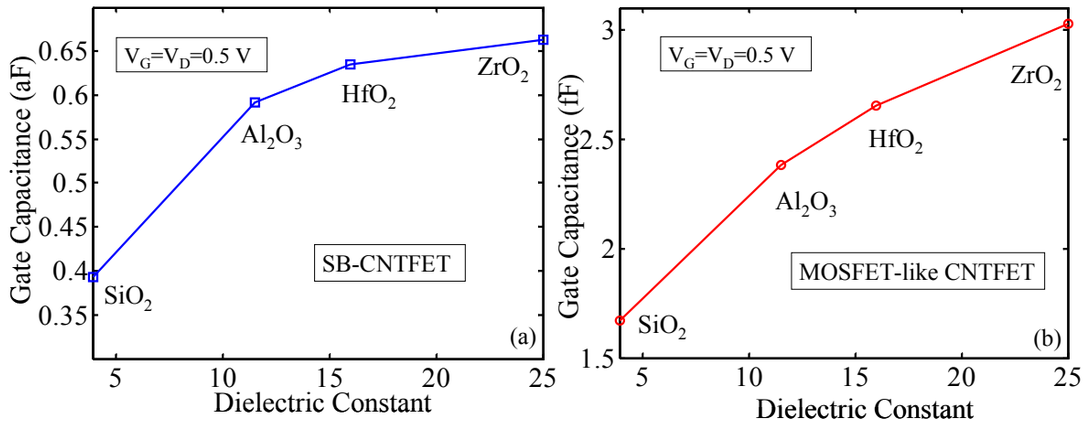

Fig. 10. Gate capacitance versus the dielectric constant a) SB-CNTFET b) MOSFET-like CNTFET.

The energy at the top of the barrier in the channel depends on the gate voltage and on the charge at the top of the barrier. When C_{ox} is small, the gate voltage controls the charge at the top of the barrier (which is independent of the drain voltage) and for large C_{ox}, the gate voltage controls the potential at the top of the barrier, which is independent of the drain

voltage (Guo and Lundstrom, 2006). In bulk devices like conventional MOSFETs, the quantum capacitance is larger than the oxide capacitance, however, CNTFETs usually work in the quantum capacitance limit (C_q<<C_{ox}).
We have compared the effect of the gate thickness on the gate capacitances of a completely gated and a partially gated SB-CNTFET. The results are shown in figure 11 and imply that the thicker gate increases C_g in the partially gated and has no effect in a completely gated SB-CNTFET (Kordrostami and Sheikhi, 2009b).

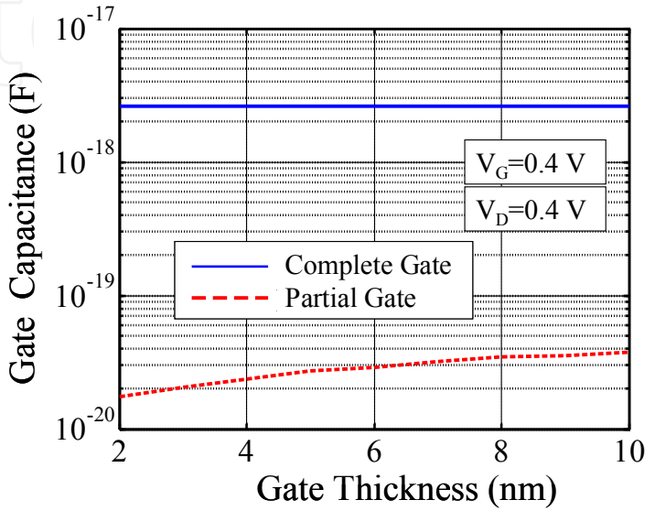

Fig. 11. Gate capacitances for two types of SB-CNTFET. The channel is an intrinsic 50 nm long (19,0) zigzag CNT, the gate length in partially gated SB-CNTFET is 5 nm and the dielectric is SiO_2 with a permittivity of 3.9.

3.6 Fringing Capacitance

The fringing fields between the gate metal and source and drain contacts result in capacitances which are called fringing or parasitic capacitances. Fringing field becomes more important when the channel length of a CNTFET is reduced. This could be comparable to the intrinsic device capacitances, and hence must be considered. In practice, appropriate electrode geometries are required to minimize the fringing field parasitic capacitances so that the parasitic capacitance due to fringing fields become negligible compared to the gate capacitance required to modulate the conductance, for example, by using 1-D metallic electrodes or nanotubes themselves as the electrodes (Yu, et al., 2006). We have investigated the effect of the contact geometry on the electrostatics of both SB-CNTFETs and MOSFET-like CNTFETs which clearly verifies the contribution of the fringing field to the device electrostatics and frequency response (kordrostami and Sheikhi, 2009a).

3.7 Cutoff Frequency

The unity current gain cutoff frequency (the frequency at which the current gain falls to unity) is usually used to describe high-frequency performance of a transistor. The cutoff frequency of the intrinsic CNTFET is called the intrinsic and the cutoff frequency of the CNTFET with inclusion of the parasitic capacitances is called the extrinsic cutoff frequency. When the parasitic capacitances are small the extrinsic cutoff frequency approaches the

intrinsic cutoff frequency. We compute the cutoff frequency (f_T) using the quasi-static approximation. The quasi-static treatment works well when the signal varies slowly compared to the time constant determined by the intrinsic gate capacitance and the channel inductance (Guo, et al., 2005). The small-signal circuit model for a CNTFET based on the quasi-static approximation, which includes the equivalent capacitive and resistive elements, but omits the equivalent inductive elements, is shown in figure 12.

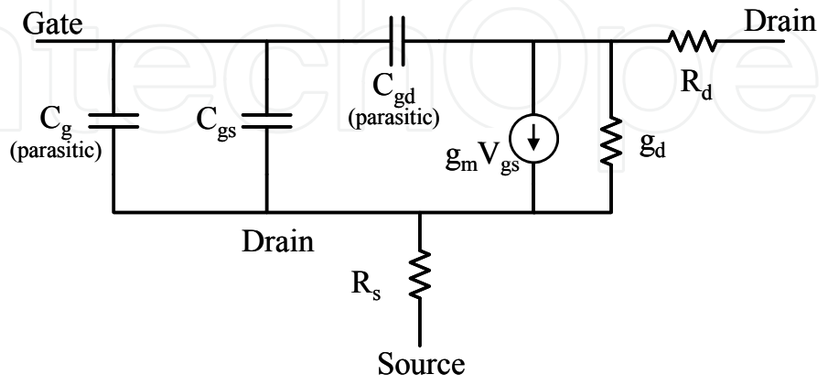

Fig. 12. Small-signal circuit model for a nanotube transistor including intrinsic and extrinsic elements.

By using the circuit model, we can generally write for the cutoff frequency:

$$\frac{1}{2\pi f_T} = (R_S + R_D)C_{gd} + \frac{1}{g_m}(C_g + C_{gs} + C_{gd}) + \frac{g_d}{g_m}(R_S + R_D)(C_g + C_{gs} + C_{gd}) \tag{4}$$

Where g_m is the transconductance, R_S and R_D are the parasitic resistances, C_g is the intrinsic gate capacitance and C_{gs} and C_{gd} are the parasitic capacitances (Burke, 2004). Calculation of the parasitic capacitances between the gate and source (drain) electrode requires separate electrostatic computations. If the parasitic resistances are excluded from the calculations we have:

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_g + C_{gs} + C_{gd}} \tag{5}$$

The cutoff frequency of the intrinsic transistor without parasitic capacitances is:

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_g} \tag{6}$$

In CNTFETs the intrinsic cutoff frequency can be determined in terms of the ratio of the change in the current to the change in the channel charge:

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_g}\Big|_{V_D=V_D(on)} = \frac{1}{2\pi}\frac{g_m}{C_g}\frac{\partial V_G}{\partial V_G} \approx \frac{1}{2\pi}\frac{\partial I_D}{\partial Q_{Ch}}\Big|_{V_D=V_D(on)} \tag{7}$$

Where, I_D is the source–drain current and Q_{Ch} is the total charge in the CNT channel and is given as (Yoon, et al., 2006):

$$Q_{Ch} = q \int_0^{L_{Ch}} N_e(x)dx \tag{8}$$

where $N_e(x)$ is the electron density as a function of the channel position and L_{Ch} is the channel length. The intrinsic cutoff frequencies of the transistors with respect to the channel length have been compared in figure 13. The shorter the channel the larger the cutoff frequency of the CNTFET.

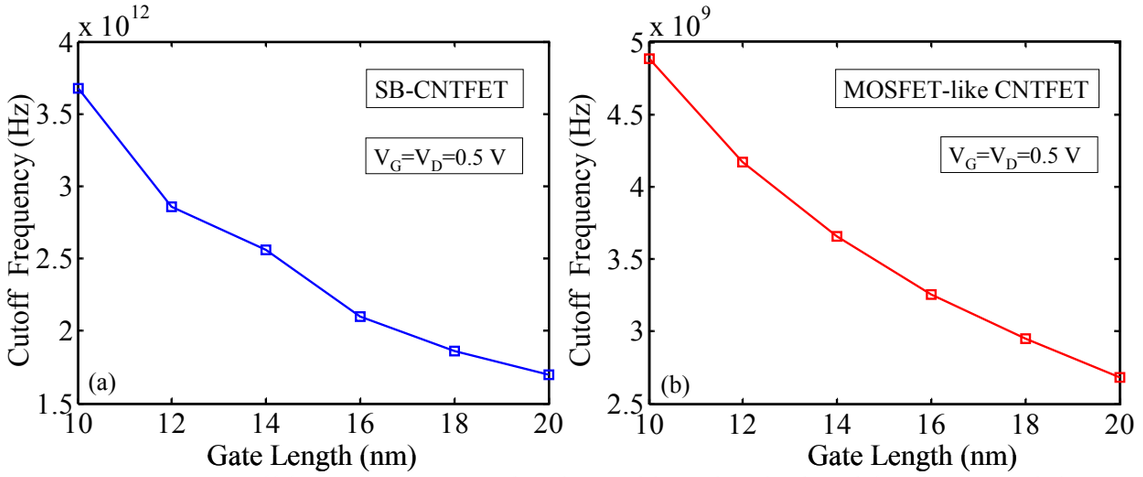

Fig. 13. Intrinsic cutoff frequency versus the channel length calculated for the typical designs in section 2.2, for a) SB-CNTFET, b) MOSFET-like CNTFET.

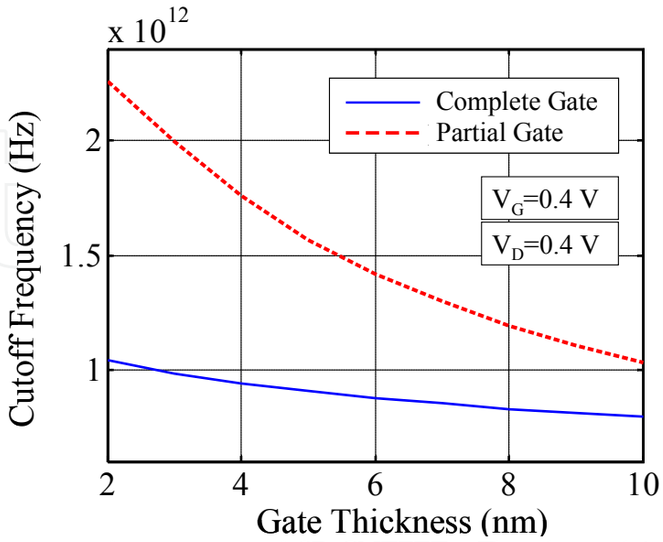

Fig. 14. Cutoff frequency of two types of SB-CNTFETs. The channel is an intrinsic 50 nm long (19,0) zigzag CNT, the gate length in partially gated SB-CNTFET is 5 nm and the dielectric is SiO_2 with a permittivity of 3.9.

From the equation 5 it can be concluded that the cutoff frequency is inversely proportional to the fringing capacitances. For example the partially gated SB-CNTFET has a higher cutoff frequency than the complete gate SB-CNTFETs because the fringing capacitances between metal electrodes are lower in partially gated SB-CNTFETs (Kordrostami and Sheikhi, 2009b). figure 14 shows the reduction of the cutoff frequency when the gate metal is thicker because of the increase of the fringing capacitances.

3.8 Intrinsic Delay

The main limitation to a faster intrinsic delay time is the gate capacitance resulting from fringing fields through the high-κ dielectric directly from the gate to source and gate to drain (Khairul and Roger, 2006). The intrinsic delay is one of the most important performance metrics for digital electronic applications and characterizes how fast a transistor switches. The switching delay can be calculated from:

$$\tau = \frac{Q_{on} - Q_{off}}{I_{On}} \tag{9}$$

Where Q_{on} is the total charge of the channel at on state ($V_G = V_{D(on)}$) and Q_{off} is the total charge of the channel at off state (V_G=0, $V_D = V_{D(on)}$) and I_{On} is the on current (Yoon, et al., 2006). The calculated intrinsic delays of the typical transistors are shown in figure 15.

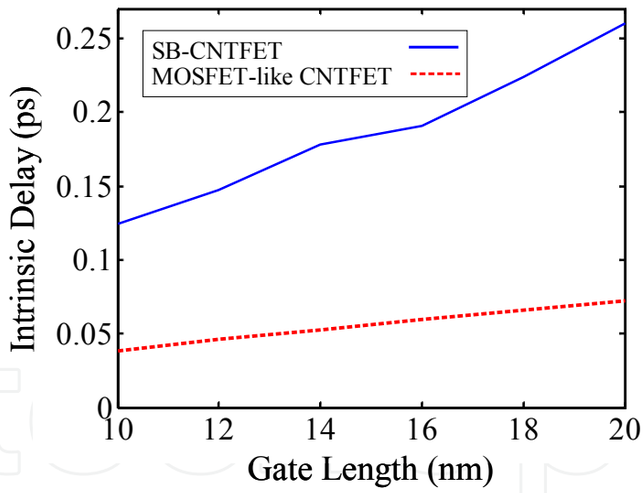

Fig. 15. Intrinsic delays of the SB-CNTFET and the MOSFET-like CNTFET versus the gate length. Longer channel length leads to larger latency. The on state is defined when V_G=V_D=0.5 V and the off state is defined as V_G=0 V and V_D=0.5 V.

4. Physical modelling of the CNTFETs

As electronic devices are being downscaled to nanometer range, the validity of the conventional modeling approaches becomes questionable. The quantitative simulation methods for nanoscale devices should incorporate an understanding of both atomistic structures and quantum mechanical effects.

In the following sections, we describe two common methodologies which can simulate the CNTFETs efficiently: NEGF formalism and WKB method for SB-CNTFETs.

4.1 NEGF Formalism

The non-equilibrium Green's function (NEGF) formalism provides a sound basis for modeling quantum devices, due to the following reasons:

- Atomic-level description of the channel.
- Channel-contact interfaces can be treated by describing open boundary conditions for the Schrödinger equation.
- Dissipative scattering processes and other phenomena like light emission can be modeled.
- Considering quantum mechanical tunneling through Schottky barriers at the metal/nanotube contacts, tunneling and reflection at barriers in the nanotube channel and band to band tunneling.

In this section, we give a brief summary of the NEGF simulation procedure and how to apply the approach to a nanotransistor. The procedure is as follows (Guo and Lundstrom, 2009):

- Identify a suitable basis set and Hamiltonian matrix (H) for an isolated channel.
- Compute the self-energy matrixes (Σ_S and Σ_D).
- Compute the retarded Green's function (G).
- Determine the physical quantities of interest from the Green's function.
- Solve NEGF transport equation iteratively with the Poisson equation until self-consistency is achieved.
- Calculate the drain current.

The procedure starts with an initial guess for the potential of the channel and then the charge density is calculated from the NEGF equations. For a given charge density, the Poisson equation is solved to obtain the electrostatic potential in the nanotube channel. Next, the computed potential profile is used as the input for the NEGF transport equation, and an improved estimate for the charge density is obtained. The iteration between the Poisson equation and the NEGF transport equation continues until self-consistency is achieved. At this time, all the physical quantities are exact and the current can be calculated. The Green's function can be calculated from:

$$G = \left[\left(E + i0^{+}\right)I - H - \Sigma_S - \Sigma_D\right]^{-1} \tag{10}$$

Where H is the Hamiltonian matrix and $\Sigma_{S,D}$ is the self energy matrixes for the source/drain interfaces. The device and the methodology are shown in figure 16.
Table 1 describes the NEGF formalism and how the physical quantities can be calculated. By choosing appropriate self-energy matrixes, the procedure can be implemented to model both types of the CNTFETs. The computationally expensive part of the procedure is calculating the Green's function. Using the real space basis set for calculation of the Hamiltonian matrix for the CNT channel leads to a matrix whose size is the total number of carbon atoms in the nanotube. In CNTFETs the mode space basis which uses the periodic boundary condition around the circumference of the nanotube is the appropriate approach

for calculation of the Hamiltonian of the channel because this approach significantly reduces the size of the Hamiltonian matrix.
After calculation of the transmission coefficient (Table 1), the current of the transistor can be computed from Landauer-Buttiker formula:

$$I = \frac{4e}{h}\int T(E)\left[f_S(E) - f_D(E)\right]dE \tag{11}$$

Where $f_{S,D}(E)$ is the Fermi function at the source/drain contact.

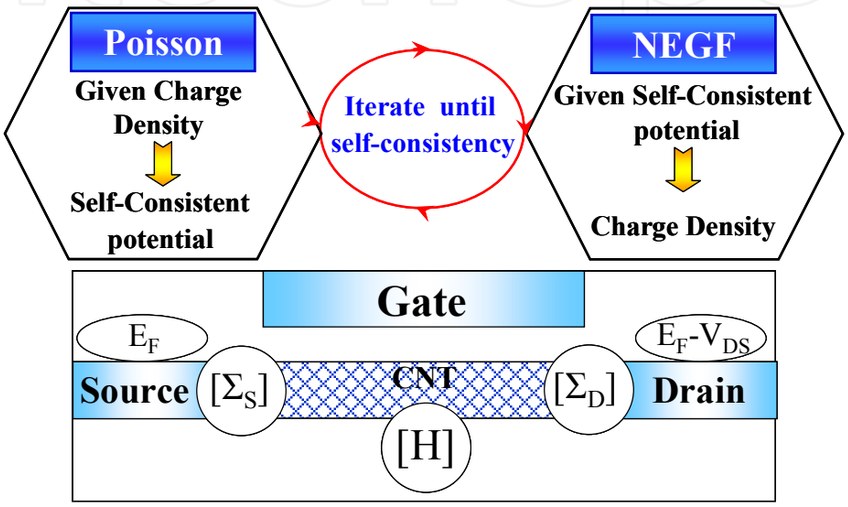

Fig. 16. The iterative method (NEGF) for calculating the potential and the charge density of the channel and the structure of the CNTFET under investigation.

Physical Quantity	Matrix Computation	Description
Broadening function	$\Gamma_S = i\left[\Sigma_S - \Sigma_S^+\right],\ \Gamma_D = i\left[\Sigma_D - \Sigma_D^+\right]$	Related to the broadened density of states in the channel.
Spectral function	$\left[A_S(E)\right] = G\Gamma_S G^+$ $\left[A_D(E)\right] = G\Gamma_D G^+$	Diagonal elements give the LDOS at energy E in that representation: $D(E) = \frac{1}{2\pi} Trace\left[A(E)\right]$
Correlation function	$[G^n(E)] = [A_S]f_S + [A_D]f_D$	The matrix version of the electron density per unit energy. From $[G^n(E)]$ density matrix can be calculated.
Density Matrix	$[\rho] = \frac{1}{2\pi}\int [G^n(E)]dE$	Diagonal elements give the electron density: $n(x) = Diag[\rho]$
Transmission Coefficient	$T(E) = Trace\left[\Gamma_S G \Gamma_D G^+\right]$	Transmission probability from source to drain.

Table 1. NEGF formalism and the description of physical quantities.

4.2 WKB Treatment of Schottky Barrier CNTFETs

The Wentzel-Kramers-Brillouin (WKB) approximation can be used to solve Schrödinger equation and find the tunneling probability at the source/drain-metal interface. This method is assumed a semi-classical approach. The channel potential distribution can be found by solving Laplace equation. The potential of the channel found from Laplace equation is valid as far as the device works in the quantum capacitance limit. At this limit, the nanotube quantum capacitance is very small and the associated accumulated charge is close to zero (Jiménez, et al., 2006). That's why the Laplace equation is valid under this condition. By using WKB method and solving Schrödinger equation, the transmission coefficient of the channel (probability of tunneling through the Schottky Barriers) is achieved which is a function of the potential energy:

$$T(E) = \exp\left[-2\int_{z_1}^{z_2} k(z)dz\right] \tag{12}$$

Where z_1 and z_2 are classical turning points and $k(z)$ is the wave number which can be calculated from:

$$k(z) = \frac{2}{3aV_0}\sqrt{\left(\frac{E_g}{2}\right)^2 - [E + eV(z)]^2} \tag{13}$$

where a = 0.144 nm, E_g = 0.83 eV and V_0 = 2.5 eV are the Carbon–Carbon bond length, the CNT band gap and the tight-binding parameter, respectively. $V(z)$ is the electrostatic potential along the CNT and is obtained by solving the Laplace equation. The computed potential profile is used as the input for the transmission coefficient and ultimately the current can be calculated from equation 11 (Kordrostami and Sheikhi, 2009c). The Schottky barrier, potential variations and the classical turning points are shown in figure 17.

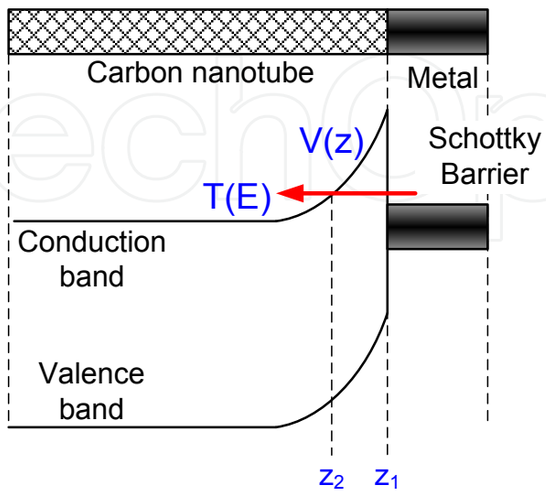

Fig. 17. Schottky barrier, potential variations near the channel-contact interface and the classical turning points which show the tunneling path.

5. Conclusion

The current-voltage characteristic of the SB-CNTFETs is ambipolar and the MOSFET-like CNTFETs exhibit unipolar characteristics. Asymmetric contact types and double gate structures are two ways for suppressing the ambipolarity of the SB-CNTFETs. Linear doping profile in MOSFET-like CNTFETs can reduce the band to band tunneling leakage current in negative voltages. High permittivity dielectrics are needed to ensure the proper control of the gate on the channel at the oxide thickness limit. The cutoff frequency of the CNTFETs severely depends on the gate and fringing capacitances. 1-D contacts can make the fringing capacitances as small as possible. Partially gated SB-CNTFET has smaller fringing capacitances and thus higher cutoff frequency in comparison with completely gated SB-CNTFET. Two simulation methodologies are reliable for modelling CNTFETs: NEGF transport equation self-consistently with Poisson equation for both types of the transistors and semi-classical WKB method for calculating the tunneling current through Schottky barriers in SB-CNTFETs. By using the simulation methods we discussed some trade-offs between different parameters of a particular CNTFET design. In order to achieve a well-designed nanotransistor, a compromise is always needed between different parameters.

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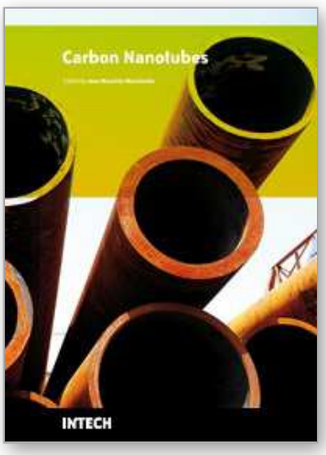

Carbon Nanotubes

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This book has been outlined as follows: A review on the literature and increasing research interests in the field of carbon nanotubes. Fabrication techniques followed by an analysis on the physical properties of carbon nanotubes. The device physics of implemented carbon nanotubes applications along with proposed models in an effort to describe their behavior in circuits and interconnects. And ultimately, the book pursues a significant amount of work in applications of carbon nanotubes in sensors, nanoparticles and nanostructures, and biotechnology. Readers of this book should have a strong background on physical electronics and semiconductor device physics. Philanthropists and readers with strong background in quantum transport physics and semiconductors materials could definitely benefit from the results presented in the chapters of this book. Especially, those with research interests in the areas of nanoparticles and nanotechnology.

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